REZA HASHEMIAN, Ph.D, P.E.

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Recent Activities: *Digital Design with FPGAs (VHDL and Verilog HDL):*

- Image/Video Compression, Huffman coding,
- Computer Arithmetic for DSP applications (High-speed adders and MACs),
- Frequency Multiplier and All Digital PLL,
- Active Noise Control,
- DSP Applications

ASIC/VLSI Design(Analog and Digital):

- Amplifiers, OTAs, Analog Multipliers, DAC, ADC and ΣΔ modulation,
- Algorithm development and Layout

EDUCATION:

Ph.D. degree in Electrical Engineering from the University of Wisconsin in Madison; Madison, Wisconsin, June 1968.

M.S. degree in Electrical Engineering from the University of Wisconsin in Madison; Madison, Wisconsin, January 1965.

B.S. degree in Electrical Engineering, Tehran University, Tehran, Iran, June 1960.

Post Doctoral:

Solar irradiation modeling; Georgia Institute of Technology, Atlanta, Georgia, Summer 1978.

Computer Aided Circuit Design; (Prof. R. Spence) Imperial College, London, England, Summer 1975.

Computer programming, logic, and Computer organization; Pennsylvania State University, University Park, Pennsylvania, Summer 1971.

RESPONSIBILITIES:

05/87 - Present - Professor in the Dept. of Electrical Engineering at Northern Illinois University, DeKalb.

Teaching: Digital and Analog IC design; Design with FPGAs and HDL; Computer aided circuit design; Electronic circuits; Design with Microprocessors/controllers.

R&D: VLSI (ASIC) design; Design with FPGA using Hardware Design Languages (VHDL and Verilog); Image/Video data compression; Design for active noise control using FPGAs; Algorithm development and design for computer arithmetic.

01/2001 – 09/2001 - Sabbatical leave at the University of Windsor, Department of Electrical and Computer Engineering, Windsor, CA., doing research.

06/94 - 01/95 - Contractor at Texas Instrument, inc. (sabbatical leave from NIU), Designs with combinations of FPGA and DSP. The work involved the design of an active periodic noise canceling system using, FPGA (ACT2 series), and design of computer arithmetic units for DSP applications.

09/91 - 05/92 - ASIC Design Engineer, Northwestern Star-Scan (FLI), Inc., 715B W. Algonquin Rd, Arlington-Heights, Illinois. In hardware design group for HDTV.

11/85 - 05/87 - Senior CAE Engineer and Section Manager; Layout Techniques for VLSI Design and Semi-custom Product Support: Signetics Corporation, Sunnyvale, California.

10/84 - 11/85 - Research Contractor; Model Development and Characterization of short channel MOS Devices: Signetics Corporation, Sunnyvale, California.

08/68 - 10/84 - Assistant, Associate, and Full Professor, Electrical Engineering Department, Sharif (former Arya Mehr) University of Technology, Tehran, Iran.

08/83 - 10/84 - Associate Provost and Director of Research and Industrial liaison, Sharif University of Technology, Tehran, Iran.

12/80 - 09/82 - Director of the "Research and Product Center", Iranian Radio and Television Association.

09/74 - 09/79 - Cofounder and Associate Director of the Materials and Energy Research Center (MERC), Sharif University of Technology, Tehran, Iran. With 124 employees MERC had four technical divisions: Solar Energy, Materials and Processes, Electronics and Computer, and Industrial Pollution.

09/71 - 09/74 - Director of the Electronics and Computer Division, MERC, Sharif University of Technology, Tehran, Iran.

07/67 - 06/68 - Instructor in the Electrical Engineering Department, University of Wisconsin, Madison, Wisconsin. Teaching electronic circuits and conducting the laboratory.

04/62 - 06/63 - Field Engineer at the Iran Electric and Water Supply Company, Tehran, Iran. Installation and test of the electric and control panels at Tehran-Shahroud Oil Pump Station.

PROFESSIONAL CONTRIBUTIONS:

* TI consultant (sabbatical leave from NIU) from July, 1994 to January, 1995; Implementation of FPGAs for: i) Design of Active Periodic Noise Control Systems, ii) High speed adders and multipliers, iii) Entropy coding using Huffman method, and iv) Customized DSP using FPGA.
* Have developed algorithm and generated specific FAX-FONT to speed up the facsimile data transmission for text using Group 3 Fax standard.
* Consultant and a member of the design team for the development of a Video Compression Decoder ASIC. The decoder utilizes four different compression techniques; namely, Direct Cosine Transformation (DCT), Vector Quantization (VQ), Sub-band Coding, and Entropy (Huffman) Coding. Other compression techniques, such as motion estimation/compensation and run-length-encoding, was also successfully implemented (09/91 - 05/92).
* Have developed new algorithms and designed numerous digital circuits and systems such as computer arithmetic units including: High speed adders/multipliers, Fast Divider, Square rooting, High speed priority encoder, Huffman coding, and Walsh-Hadamard Transformation Processor, (02/88 - 06/92).
* Developed digital systems using digital signal processors and microcontrollers; DSP56000, DSP96000, and 80C196 chip. The microcontroller 80C196 was specifically used in PINSET (blood sugar measurement test) project, sponsored by Safety Diagnostics, Inc., Evanston, Illinois (03/90 - 02/91).
* Major contributor in the development of a switch level logic simulator (LOGICSIM) with graphic schematic capture capability (09/89 - 05/92).
* Developed and implemented new strategies and techniques for standard cell, and block placement and routing (12/85 - 05/87).
* Modified MOSPAR program; a software package for modeling and characterization of short channel MOS devices. A new model with very high accuracy in the sub-threshold region was developed for short channel MOS devices (11/84 - 11/85).
* The principal investigator in the research project, contracted between Simens AG Company, Munich, Germany, and Sharif University of Technology, Tehran, Iran. The project was aimed to conduct research related to the MOS transistor modeling and characterization, mainly for the design of FAMOS memory cells (1972-1975).
* In charge of design and development of the "Program for Analysis and Design of General Active Networks" (PADGAN). PADGAN, with interactive graphic capability, contained built-in models for both bipolar and MOS transistors. The program was capable of doing the following analysis: operating point, time domain, and frequency domain. Both large and small sensitivity analysis were included in the program. Pole/zero, allocation in conjunction with the sensitivity analysis played an important role in the design. Sparse LU factorization was also implemented for speedy analysis (1973-1978). PADGAN was doing a great job at the time that SPICE was not fully developed and commonly accessible.
* In charge of design and development of a program for computation of heating load and cooling load of buildings. The program utilized a Table Look Up for the heat coefficients and heat capacitance of the appropriate building materials. Given a building structure with materials being used, the program would construct an equivalent electrical model for the heat flow and the heat storage capacities in the structure. Then a performance analysis would have been followed (1978-1979).
* Design, development, and construction of a microcomputer unit in chip level, using 8080 processor. The unit was aimed toward education of basic, logical analysis and hardware design purposes (1982-1983).
* Co-founder of the Materials and Energy Research Center (MERC); 1971.
* One of the founders of SHARIF monthly newspaper. SHARIF is an academic, research and development newspaper published in Iran; 1983.
* Hold a patent on bilingual display monitor (Iran 1976), Have filed a patent on All Digital Frequency Multiplier (NIU, 1996), and have sixty papers published, or contributed at the professional conferences. Co-authored a text book on Pulse Technique.

MEMBERSHIP:

* Holder of Professional Engineering Registration (PE) from the state of Illinois (October 1992).
* life Member of IEEE
* Member of the first executive committee of IEEE, Iran Section,1970-1972
* Member of Tau Beta Phi and Eta Kappa Nu

Programming Languages: Most programming and design languages (Fortran, Pascal, Visual Basic, C++, Java, Assembly, Verilog, VHDL).

PUBLICATIONS (last several years):

* R. Hashemian, "Local Biasing and the Use of Nullator-Norator Pairs in Analog Circuits ", Proceedings of the 2008 IEEE International Midwest Symposium On Circuits And Systems, Knoxville, TN, August 10 - 13, 2008.
* R. Hashemian, "Use of Local Biasing in Designing Analog Integrated Circuits", 2008 IEEE International Conference on Electro/Information Technology EIT2008, Ames, Iowa, May 18 – 20, 2008.
* R. Hashemian, "A Method to Design, Construct and Test Digital Hardware all in Classroom Environment", Proceedings of the FIE2007 Conference, Milwaukee, Wisc., October 11 - 13, 2007.
* R. Hashemian, "FPGA e-Lab, a Technique to Remoe Access a Laboratory to Design and Test", IEEE International Conference on Microelectronic System Education, San Diago, Ca., 3 – 4 June, 2007.
* R. Hashemian, "A Linear-like Biasing Technique forNonlinear Circuits", Proceedings of the International Conference on Integrated Circuit Design & Technology, Austin, Texas; May 30 – June 1, 2007.
* R. Hashemian, "Partial Local Biasing, A New Method to Modify/Tune Amplifiers for a Desirable Performance", 2007 IEEE International Conference on Electro/Information Technology, IIT, Chicago, May 17 – 19, 2007.
* R. Hashemian, "Designing Analog Circuits with Reduced Biasing Power", Proceedings of the 13th IEEE International Conference on Electronics, Circuits and Systems, Nice, France Dec. 10– 13, 2006
* R. Hashemian, "New Analysis and Design Technique for Analog Circuits ", Proceedings of the 2006 IEEE International Midwest Symposium On Circuits And Systems, San Juan, Puerto Rico, August 6 – 9, 2006.
* R. Hashemian, "Analog Circuit Design with Linearized DC Biasing ", Proceedings of the 2006 IEEE International Conference on Electro/Information Technology, Michigan State University; Lancing ,MI, May 7– 10, 2006.
* R. Hashemian, "Teaching an Introductory Engineering Course to Help Students to Better Select Their Majors", Proceedings of the FIE2005 Conference, Indianapolis, Indiana, October 19 - 22, 2005.
* R. Hashemian, "Port Nullification, A Methodology To Simulate With Nonlinear Devices ", Proceedings of the 48th IEEE International Midwest Symposium On Circuits And Systems, Cincinnati, OH, August 7 – 10, 2005.
* R. Hashemian, "Use of Conditional Additivity in Circuits with Exponential Nonlinearities", Proceedings of the 48th IEEE International Midwest Symposium On Circuits And Systems, Cincinnati, OH, August 7 – 10, 2005.
* R. Hashemian and Chandi Pedapati " Backboard-Based Digital Hardware Design Using FPGAs ", Proceedings of ASEE, 2005 IL/IN Sectional Conference, Section B-T3-4, April 1-2, 2005.
* R. Hashemian " A Method to Teach an Introductory Engineering course ", Proceedings of ASEE, 2005 IL/IN Sectional Conference, Section C-T1-3, April 1-2, 2005.
* R. Hashemian, " Condensed Table of Huffman Coding, A New Approach to Efficient Coding ", IEEE Trans. on Communications, Vol. 52, no. 1, pp 6 – 8, January 2004.
* R. Hashemian, and Bipin Sereedharan" A Hybrid Number System and its Application in FPGA-DSP Teaching ", IEEE International Conference on Information Technology (ITCC 2004), at Las Vegas, Nevada, pp 342 – 346, April 5 – 7, 2004.
* R. Hashemian, M. Sathya Marivada, " Improved Image Compression Using Fractal Block Coding ", Proceedings of the 46th IEEE International Midwest Symposium on Circuits and Systems, Cairo, Egypt, December 27 - 30, 2003.
* R. Hashemian, " Direct Huffman Coding Using Table Of Code Lengths ", IEEE International Conference on Information Technology (ITCC 2003), at Las Vegas, Nevada, April 28 – 30, 2003.
* R. Hashemian, et al, " A B-s Complement Continuous Valued Digit Adder ", IEEE International Symposium on Circuits and Systems (ISCAS 2002), at Fairmont Scottsdale, Scottsdale, AZ, May 25 – 29, 2002.
* R. Hashemian, " CONDENCED HUFFMAN CODING, A NEW EFFICIENT DECODING TECHNIQUE ", Proceedings of the IEEE Midwest Symposium on Circuits and Systems (MWSCAS-45), Tulsa, OK, August 4 - 7, 2002.

* R. Hashemian, M. Ahmadi, " Efficient Resource Allocation and Higher Speed for Image Decoders ", IEEE MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS (MWSCAS 2001), at Dayton, Ohio, August 14 – 17, 2001.
* R. Hashemian, et al, " Application of 2-D Filtering in Determination of the Velocity of Flow Fields ", IEEE Pacific Rim Conference on Communication Computers and Signal Processing (PACRIM 2001), at the University of Victoria, Victoria, B.C., August 26 – 28, 2001.
* R. Hashemian, et al, " Design of High Throughput 2-D FIR Filters Using Singular Value Decomposition (SVD) and Genetic Algorithms ", IEEE Pacific Rim Conference on Communication Computers and Signal Processing (PACRIM 2001), at the University of Victoria, Victoria, B.C., August 26 – 28, 2001.
* R. Hashemian, M. Ahmadi, " Reduced Code Transmission and High Speed Reconstruction of Huffman Tables ", IEEE Pacific Rim Conference on Communication Computers and Signal Processing (PACRIM 2001), at the University of Victoria, Victoria, B.C., August 26 – 28, 2001.
* R. Hashemian, "A New Design for High Speed and High-Density Carry Select Adders", 43rd Midwest Symposium on Circuits and Systems, Lansing, Michigan, August 8-11, 2000.
* R. Hashemian, S. Vijayaraghavan, and James Citta, "A Low Gate Image Encoder", 42nd Midwest Symposium on Circuits and Systems, New Mexico State University, Las Cruces, August 8-11, 1999.
* R. Hashemian, Felipe Hernandez, and James Citta, "A New Algorithm and Design for a Low Gate Still Image Encoder", The 7th Annual Conference on Electrical Engineering, ICEE'99, May12-15, 1999.
* R. Hashemian, "A New English to Persian Type-Script Conversion Package", The 3rd IAA Annual Conference "Computer and Communication", September 19-20, 1998.
* R. Hashemian, and James Citta, "Design and Hardware Implementation of a New Image Encoder Using FPGA Technology", The 3rd IAA Annual Conference "Computer and Communication", September 19-20, 1998.
* R. Hashemian, "Memory Efficient and High Speed Search Huffman Coding", IEEE Trans. on Communications, IECMBT, vol.43, no.10, pp.2576-2581, October, 1995.
* R. Hashemian, "Design and Hardware Implementation of a Memory Efficient Huffman Decoding", IEEE Trans. on Consumer Electronics, vo.40, no.3, pp.345-352, August, 1994.
* R. Hashemian, "Acoustic Noise Control System Design", The Fifth Iranian Conference on Electrical Engineering, Tehran, Iran, Mat 6-8, 1997
* R. Hashemian, "Fast Addition Using a New Number", 30th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, November 3-6, 1996.
* R. Hashemian, "A New Number Method for Conversion of a 2's Complement to Canonic Signed Digit Number System and its Representation", 30th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, November 3-6, 1996.
* R. Hashemian, "A New Number System for Fast Multiplication", Midwest Symposium on Circuits and Systems, Ames, Iowa, August 18-21, 1996.
* R. Hashemian, "Efficient Variable-Length Coding Under an Assigned Maximum Code-Length Constraint," IEEE International Symposium on Circuits and Systems (ISCAS 96), Atlanta, Georgia, May, 1996.
* R. Hashemian, "Active Periodic Noise Control Using a Single FPGA Chip", IEEE International Conference on Consumer Electronics, ICCE'95, Chicago, Illinois, June 7-9, 1995.
* R. Hashemian, "Design of an Active Noise Control System Using Combinations of DSP and FPGAs", PLDCon'95 Conference, Santa Clare, CA, April 25-27, 1995.
* R. Hashemian, "Fast Carry Adder Using FPGA Technology", 37th IEEE Midwest Symposium on Circuits and Systems, Lafayette, Louisiana, August 3-5, 1994.
* R. Hashemian, "An Algorithm for the Design of a 54-bit Adder Using a Modified Manchester Carry Chain", Proceedings of the Forth Grate Lakes Symposium on VLSI, March 1994.
* R. Hashemian, "Design and Hardware Construction of a High Speed and Memory Efficient Huffman Decoding", Proceedings of the IEEE/ICCE Conference, Chicago, IL, June 21-23, 1994.
* R. Hashemian, K. Golla, S.M. Kuo, and A. Joshi, "Design and Construction of an Active Periodic Noise Canceling System Using FPGAs," 36th IEEE Midwest Symposium on Circuits and Systems, Detroit, MI, August 16-18, 1993.
* R. Hashemian, "A New Algorithm to Construct Parallel Adder for High Density Codes," 36th IEEE Midwest Symposium on Circuits and Systems, Detroit, MI, August 16-18, 1993.
* R. Hashemian, "A Speed-Area Efficient Algorithm for Huffman Decoding," ICEE'93 Iranian Conference on Electrical Engineering, Tehran, Iran, May 18-21, 1993.
* R. Hashemian, "High Speed Search and Memory Efficient Huffman Coding," 1993 IEEE International Symposium on Circuits and Systems, Chicago Illinois, May 3-6 1993.